

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Nam-Jung HER, et al.

Serial No.: 10/803,792

Examiner: Radosevich, Steven D.

Filed: March 17, 2004

Group Art Unit: 2117

Confirmation No.: 5596

For: SEMICONDUCTOR INTEGRATED CIRCUIT HAVING A NUMBER
OF DATA OUTPUT PINS CAPABLE OF SELECTIVELY PROVIDING
OUTPUT SIGNALS AND TEST METHOD THEREOF

Date: November 28, 2007

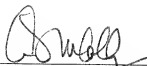
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**APPLICANT'S COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR
ALLOWANCE**

Although the Examiner's statement quotes most of the limitations of the independent apparatus claim, patentability of the claimed invention should be considered as a whole. And the invention is as defined in the claims, not as characterized by the Examiner. Finally, although not mentioned by the Examiner, the method claims and dependent apparatus claims each include additional patentable limitations that further define the invention.

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Respectfully submitted,
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